| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 07:59 |
| 2 | 2030 | ((leaf or module or tiles) near4 cell) and horizontal and vertical | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:15 |
| 3 | 669 | (((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:00 |
| 4 | 0 | ((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and bitcell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:01 |
| 5 | 331 | ((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:01 |
| 6 | 293 | (((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:12 |
| 7 | 64 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and netlist | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:03 |
| 8 | 0 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and parametric | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:13 |
| 9 | 155 | hierarchical$4 near4 (arrange or stitch$3) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:17 |
| 10 | 0 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and (hierarchical$4 near4 (arrange or stitch$3)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:17 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 1 | ☒ | ☐ | US 6493658 B1 | 20021210 | 88 | Optimization processing for integrated circuit physical design automation system using optimally switched fitness improvement algorithms | 703/1 |
| 2 | ☐ | ☐ | US 6490717 B1 | 20021203 | 32 | Generation of sub-netlists for use in incremental compilation | 716/18 |
| 3 | ☐ | ☐ | US 6421818 B1 | 20020716 | 80 | Efficient top-down characterization method | 716/18 |
| 4 | ☒ | ☐ | US 6407434 B1 | 20020618 | 136 | Hexagonal architecture | 257/401 |
| 5 | ☒ | ☐ | US 6378123 B1 | 20020423 | 81 | Method of handling macro components in circuit design synthesis | 716/18 |
| 6 | ☐ | ☐ | US 6357035 B1 | 20020312 | 6 | Method and apparatus for the automated generation of programmable interconnect matrices | 716/11 |
| 7 | ☐ | ☐ | US 6324678 B1 | 20011127 | 45 | Method and system for creating and validating low level description of electronic design | 716/18 |
| 8 | ☒ | ☐ | US 6312980 B1 | 20011106 | 134 | Programmable triangular shaped device having variable gain | 438/197 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 9 | ☒ | ☐ | US 6295636 B1 | 20010925 | 82 | RTL analysis for improved logic synthesis | 716/18 |
| 10 | ☒ | ☐ | US 6292931 B1 | 20010918 | 81 | RTL analysis tool | 716/18 |
| 11 | ☒ | ☐ | US 6289498 B1 | 20010911 | 81 | VDHL/Verilog expertise and gate synthesis automation system | 716/18 |
| 12 | ☒ | ☐ | US 6289491 B1 | 20010911 | 80 | Netlist analysis tool by degree of conformity | 716/5 |
| 13 | ☒ | ☐ | US 6263483 B1 | 20010717 | 81 | Method of accessing the generic netlist created by synopsys design compilier | 716/18 |
| 14 | ☐ | ☐ | US 6243849 B1 | 20010605 | 9 | Method and apparatus for netlist filtering and cell placement | 716/8 |
| 15 | ☐ | ☐ | US 6216252 B1 | 20010410 | 53 | Method and system for creating, validating, and scaling structural description of electronic device | 716/1 |
| 16 | ☒ | ☐ | US 6209123 B1 | 20010327 | 114 | Methods of placing transistors in a circuit layout and semiconductor device with automatically placed transistors | 716/14 |
| 17 | ☒ | ☐ | US 6205572 B1 | 20010320 | 79 | Buffering tree analysis in mapped design | 716/5 |
| 18 | ☐ | ☐ | US 6195788 B1 | 20010227 | 21 | Mapping heterogeneous logic elements in a programmable logic device | 716/18 |
| 19 | ☒ | ☐ | US 6173435 B1 | 20010109 | 80 | Internal clock handling in synthesis script | 716/18 |
| 20 | ☒ | ☐ | US 6173434 B1 | 20010109 | 13 | Dynamically-configurable digital processor using method for relocating logic array modules | 716/17 |
| 21 | ☐ | ☐ | US 6155725 A | 20001205 | 84 | Cell placement representation and transposition for integrated circuit physical design automation system | 716/9 |
| 22 | ☒ | ☐ | US 6134705 A | 20001017 | 32 | Generation of sub-netlists for use in incremental compilation | 716/18 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 23 | ☐ | ☐ | US 6102964 A | 20000815 | 24 | Fitting for incremental compilation of electronic designs | 716/18 |
| 24 | ☒ | ☐ | US 6097073 A | 20000801 | 138 | Triangular semiconductor or gate | 257/401 |
| 25 | ☒ | ☐ | US 6006024 A | 19991221 | 112 | Method of routing an integrated circuit | 716/12 |
| 26 | ☒ | ☐ | US 5987086 A | 19991116 | 113 | Automatic layout standard cell routing | 716/1 |
| 27 | ☒ | ☐ | US 5984510 A | 19991116 | 113 | Automatic synthesis of standard cell layouts | 716/2 |
| 28 | ☒ | ☐ | US 5973376 A | 19991026 | 136 | Architecture having diamond shaped or parallelogram shaped cells | 257/401 |
| 29 | ☒ | ☐ | US 5963975 A | 19991005 | 84 | Single chip integrated circuit distributed shared memory (DSM) and communications nodes | 711/147 |
| 30 | ☒ | ☐ | US 5914887 A | 19990622 | 84 | Congestion based cost factor computing apparatus for integrated circuit physical design automation system | 716/8 |
| 31 | ☒ | ☐ | US 5903461 A | 19990511 | 67 | Method of cell placement for an integrated circuit chip comprising chaotic placement and moving windows | 700/121 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 32 | ☒ | ☐ | US 5889329 A | 19990330 | 139 | Tri-directional interconnect architecture for SRAM | 257/758 |
| 33 | ☒ | ☐ | US 5875117 A | 19990223 | 84 | Simultaneous placement and routing (SPAR) method for integrated circuit physical design automation system | 716/14 |
| 34 | ☒ | ☐ | US 5872380 A | 19990216 | 136 | Hexagonal sense cell architecture | 257/369 |
| 35 | ☒ | ☐ | US 5870313 A | 19990209 | 84 | Optimization processing for integrated circuit physical design automation system using parallel moving windows | 716/10 |
| 36 | ☒ | ☐ | US 5870308 A | 19990209 | 49 | Method and system for creating and validating low-level description of electronic design | 716/18 |
| 37 | ☒ | ☐ | US 5864165 A | 19990126 | 141 | Triangular semiconductor NAND gate | 257/401 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 38 | ☒ | ☐ | US 5834821 A | 19981110 | 140 | Triangular semiconductor "AND" gate device | 257/401 |
| 39 | ☒ | ☐ | US 5822214 A | 19981013 | 135 | CAD for hexagonal architecture | 716/10 |
| 40 | ☒ | ☐ | US 5818729 A | 19981006 | 23 | Method and system for placing cells using quadratic placement and a spanning tree model | 716/9 |
| 41 | ☒ | ☐ | US 5815403 A | 19980929 | 83 | Fail-safe distributive processing method for producing a highest fitness cell placement for an integrated circuit chip | 716/9 |
| 42 | ☒ | ☐ | US 5811863 A | 19980922 | 136 | Transistors having dynamically adjustable characteristics | 257/401 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 43 | ☒ | ☐ | US 5808330 A | 19980915 | 136 | Polydirectional non-orthoginal three layer interconnect architecture | 257/208 |
| 44 | ☒ | ☐ | US 5801958 A | 19980901 | 95 | Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information | 716/18 |
| 45 | ☒ | ☐ | US 5801422 A | 19980901 | 139 | Hexagonal SRAM architecture | 257/369 |
| 46 | ☒ | ☐ | US 5793644 A | 19980811 | 84 | Cell placement alteration apparatus for integrated circuit chip physical design automation system | 716/2 |
| 47 | ☒ | ☐ | US 5789770 A | 19980804 | 136 | Hexagonal architecture with triangular shaped cells | 257/206 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 48 | ☒ | ☐ | US 5781439 A | 19980714 | 83 | Method for producing integrated circuit chip having optimized cell placement | 700/121 |
| 49 | ☒ | ☐ | US 5777360 A | 19980707 | 137 | Hexagonal field programmable gate array architecture | 257/315 |
| 50 | ☒ | ☐ | US 5745363 A | 19980428 | 83 | Optimization processing for integrated circuit physical design automation system using optimally switched cost function computations | 700/121 |
| 51 | ☒ | ☐ | US 5742510 A | 19980421 | 83 | Simultaneous placement and routing (SPAR) method for integrated circuit physical design automation system | 700/97 |
| 52 | ☒ | ☐ | US 5742086 A | 19980421 | 136 | Hexagonal DRAM array | 257/300 |
| 53 | ☒ | ☐ | US 5682322 A | 19971028 | 83 | Optimization processing for integrated circuit physical design automation system using chaotic fitness improvement method | 716/2 |
| 54 | ☒ | ☐ | US 5636125 A | 19970603 | 66 | Computer implemented method for producing optimized cell placement for integrated circiut chip | 700/121 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 55 | ☒ | ☐ | US 5598344 A | 19970128 | 51 | Method and system for creating, validating, and scaling structural description of electronic device | 716/18 |
| 56 | ☒ | ☐ | US 5572436 A | 19961105 | 48 | Method and system for creating and validating low level description of electronic design | 716/18 |
| 57 | ☒ | ☐ | US 5557533 A | 19960917 | 67 | Cell placement alteration apparatus for integrated circuit chip physical design automation system | 716/9 |
| 58 | ☒ | ☐ | US 5557531 A | 19960917 | 47 | Method and system for creating and validating low level structural description of electronic design from higher level, behavior-oriented description, including estimating power dissipation of physical implementation | 716/1 |
| 59 | ☒ | ☐ | US 5555201 A | 19960910 | 95 | Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information | 716/1 |
| 60 | ☒ | ☐ | US 5553002 A | 19960903 | 47 | Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, using milestone matrix incorporated into user-interface | 716/11 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 61 | ☒ | ☐ | US 5544066 A | 19960806 | 47 | Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of low-level design constraints | 716/18 |
| 62 | ☒ | ☐ | US 5541849 A | 19960730 | 46 | Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including estimation and comparison of timing parameters | 716/18 |
| 63 | ☒ | ☐ | US 5495419 A | 19960227 | 80 | Integrated circuit physical design automation system utilizing optimization process decomposition and parallel processing | 700/121 |
| 64 | ☒ | ☐ | US 5487018 A | 19960123 | 13 | Electronic design automation apparatus and method utilizing a physical information database | 716/11 |

| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| - | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| - | 4 | ((((leaf or module or tiles) near4 cell) and parametric) and (input/output or I/O)) and netlist | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/08 16:26 |
| - | 35 | (((leaf or module or tiles) near4 cell) and parametric) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/08 16:53 |
| - | 93 | ((leaf or module or tiles) near4 cell) and parametric | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 07:59 |
| - | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 07:59 |
| - | 2030 | ((leaf or module or tiles) near4 cell) and horizontal and vertical | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:30 |
| - | 669 | (((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:00 |
| - | 0 | ((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and bitcell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:01 |
| - | 331 | ((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:31 |
| - | 64 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and netlist | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:27 |
| - | 0 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and parametric | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:13 |
| - | 155 | hierarchical$4 near4 (arrange or stitch$3) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| - | 0 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and (hierarchical$4 near4 (arrange or stitch$3)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:17 |

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|---|---|---|---|---|
| - | 293 | (((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:27 |
| - | 199 | ((leaf or module or tiles) near4 cell) same (horizontal and vertical) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:30 |
| - | 45 | (((leaf or module or tiles) near4 cell) same (horizontal and vertical)) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 09:08 |
| - | 4202261 | bitcell or (flip adj flop) or (store ajd element) register | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:12 |
| - | 41844 | (bitcell or (flip adj flop) or (store ajd element) or register) adj2 array | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:25 |
| - | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:27 |
| - | 304 | ((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:16 |
| - | 916 | hierarchical$4 near4 (arrange or stitch$3 or interconnect$5) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:14 |
| - | 4 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:14 |
| - | 11 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (global adj4 signal) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:19 |
| - | 70 | ((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:23 |
| - | 4 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5))) and ((leaf or module or tiles) near4 cell) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 12:03 |
| - | 45458 | (bitcell or (flip adj flop) or (storage ajd element) or register) adj2 array | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:26 |
| - | 339 | ((bitcell or (flip adj flop) or (storage ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:26 |

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| - | 4 | (((bitcell or (flip adj flop) or (storage ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:26 |
| - | 16008 | (leaf or module or tile) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:28 |
| - | 0 | ((((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (global adj4 signal)) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 12:03 |

| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 3 | 4202261 | bitcell or (flip adj flop) or (store ajd element) register | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:12 |
| 4 | 41844 | (bitcell or (flip adj flop) or (store ajd element) or register) adj2 array | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:25 |
| 5 | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| 6 | 304 | ((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:16 |
| 7 | 916 | hierarchical$4 near4 (arrange or stitch$3 or interconnect$5) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:14 |
| 8 | 4 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:14 |
| 9 | 11 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (global adj4 signal) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:19 |
| 10 | 70 | ((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:23 |
| 12 | 4 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5))) and ((leaf or module or tiles) near4 cell) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:23 |
| 13 | 45458 | (bitcell or (flip adj flop) or (storage ajd element) or register) adj2 array | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:26 |
| 14 | 339 | ((bitcell or (flip adj flop) or (storage ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:26 |
| 15 | 4 | (((bitcell or (flip adj flop) or (storage ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:26 |

| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 3 | 4202261 | bitcell or (flip adj flop) or (store ajd element) register | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:12 |
| 4 | 41844 | (bitcell or (flip adj flop) or (store ajd element) or register) adj2 array | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| 5 | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| 6 | 304 | ((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:16 |
| 7 | 916 | hierarchical$4 near4 (arrange or stitch$3 or interconnect$5) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:14 |
| 8 | 4 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:14 |
| 9 | 11 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (global adj4 signal) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:19 |
| 10 | 70 | ((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:20 |
| - | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| - | 4 | ((((leaf or module or tiles) near4 cell) and parametric) and (input/output or I/O)) and netlist | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/08 16:26 |
| - | 35 | (((leaf or module or tiles) near4 cell) and parametric) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/08 16:53 |
| - | 93 | ((leaf or module or tiles) near4 cell) and parametric | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 07:59 |
| - | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 07:59 |

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|---|---|---|---|---|
| - | 2030 | ((leaf or module or tiles) near4 cell) and horizontal and vertical | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:30 |
| - | 669 | (((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:00 |
| - | 0 | ((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and bitcell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:01 |
| - | 331 | ((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:31 |
| - | 64 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and netlist | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:27 |
| - | 0 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and parametric | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:13 |
| - | 155 | hierarchical$4 near4 (arrange or stitch$3) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| - | 0 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and (hierarchical$4 near4 (arrange or stitch$3)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:17 |
| - | 293 | (((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:27 |
| - | 199 | ((leaf or module or tiles) near4 cell) same (horizontal and vertical) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:30 |
| - | 45 | (((leaf or module or tiles) near4 cell) same (horizontal and vertical)) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 09:08 |

| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 3 | 4202261 | bitcell or (flip adj flop) or (store ajd element) register | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:12 |
| 4 | 41844 | (bitcell or (flip adj flop) or (store ajd element) or register) adj2 array | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| 5 | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:13 |
| 6 | 304 | ((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:16 |
| 7 | 916 | hierarchical$4 near4 (arrange or stitch$3 or interconnect$5) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:14 |
| 8 | 4 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:14 |
| 9 | 11 | (((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and ((leaf or module or tiles) near4 cell)) and (global adj4 signal) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:19 |
| 10 | 70 | ((bitcell or (flip adj flop) or (store ajd element) or register) adj2 array) and (hierarchical$4 near4 (arrange or stitch$3 or interconnect$5)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 11:20 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 1 | ☐ | ☐ | US 20010052062 A1 | 20011213 | 57 | PARALLEL COMPUTER WITHIN DYNAMIC RANDOM ACCESS MEMORY | 712/32 |
| 2 | ☐ | ☐ | US 6212668 B1 | 20010403 | 15 | Gain matrix for hierarchical circuit partitioning | 716/7 |
| 3 | ☒ | ☐ | US 5777608 A | 19980707 | 51 | Apparatus and method for in-parallel scan-line graphics rendering using content-searchable memories | 345/519 |
| 4 | ☒ | ☐ | US 5758148 A | 19980526 | 31 | System and method for searching a data base using a content-searchable memory | 707/6 |

| | U | 1 | Document ID | Issue Date | Pages | Title | Current OR |
|---|---|---|---|---|---|---|---|
| 1 | ☒ | ☐ | US 20030001634 A1 | 20030102 | 18 | Delay compensation circuit | 327/158 |
| 2 | ☐ | ☐ | US 6353921 B1 | 20020305 | 23 | Hardwire logic device emulating any of two or more FPGAs | 716/17 |
| 3 | ☐ | ☐ | US 6226779 B1 | 20010501 | 23 | Programmable IC with gate array core and boundary scan capability | 716/16 |
| 4 | ☒ | ☐ | US 6134517 A | 20001017 | 24 | Method of implementing a boundary scan chain | 703/28 |
| 5 | ☒ | ☐ | US 6120551 A | 20000919 | 24 | Hardwire logic device emulating an FPGA | 716/17 |
| 6 | ☐ | ☐ | US 6071314 A | 20000606 | 25 | Programmable I/O cell with dual boundary scan | 716/17 |
| 7 | ☒ | ☐ | US 5991908 A | 19991123 | 24 | Boundary scan chain with dedicated programmable routing | 714/727 |
| 8 | ☒ | ☐ | US 5926036 A | 19990720 | 51 | Programmable logic array circuits comprising look up table implementation of fast carry adders and counters | 326/40 |
| 9 | ☒ | ☐ | US 5828229 A | 19981027 | 47 | Programmable logic array integrated circuits | 326/40 |
| 10 | ☒ | ☐ | US 5790539 A | 19980804 | 27 | ASIC chip for implementing a scaleable multicast ATM switch | 370/390 |
| 11 | ☒ | ☐ | US 5535408 A | 19960709 | 43 | Processor chip for parallel processing system | 712/16 |

| | Current XRef | Retrieval Classif | Inventor | S | C | P | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | | | Cao, Xianguo et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 2 | 257/210; 716/12; 716/16 | | Law, Edwin S. et al. | ☒ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 3 | 326/16; 326/47; 714/30; 714/727; 714/733 | | Baxter, Glenn A. et al. | ☒ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 4 | 714/727 | | Baxter, Glenn A. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 5 | | | Law, Edwin S. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 6 | 326/16; 326/47; 714/30; 714/727; 714/733; 716/16; 716/8 | | Baxter, Glenn A. et al. | ☒ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 7 | 716/16 | | Baxter, Glenn A. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 8 | 326/39; 326/41 | | Cliff, Richard G. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 9 | 326/38 | | Cliff, Richard G. et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 10 | 370/398 | | Chao, Hung-Hsiang Jonathan et al. | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |
| 11 | 710/52; 711/106; 712/13 | | Hillis, W. Daniel | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ | ☐ |

| L Number | Hits | Search Text | DB | Time stamp |
|---|---|---|---|---|
| 1 | 16008 | (leaf or module or tiles) near4 cell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 07:59 |
| 2 | 2030 | ((leaf or module or tiles) near4 cell) and horizontal and vertical | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:30 |
| 3 | 669 | (((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:00 |
| 4 | 0 | ((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and bitcell | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:01 |
| 5 | 331 | ((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:31 |
| 7 | 64 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and netlist | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:27 |
| 8 | 0 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and parametric | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:13 |
| 9 | 155 | hierarchical$4 near4 (arrange or stitch$3). interconnect | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:17 |
| 10 | 0 | ((((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal) and (hierarchical$4 near4 (arrange or stitch$3)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:17 |
| 6 | 293 | (((((leaf or module or tiles) near4 cell) and horizontal and vertical) and memory) and (input/output or I/O)) and signal | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:27 |
| 11 | 199 | ((leaf or module or tiles) near4 cell) same (horizontal and vertical) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:30 |
| 12 | 45 | (((leaf or module or tiles) near4 cell) same (horizontal and vertical)) and (input/output or I/O) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB | 2003/08/09 08:31 |